

What is claimed is:

1. A method of operating a flash memory comprising:
 - copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory;
 - performing a write operation to write second data to the first array bank in response to an external processor coupled to the flash memory;
 - reading the first data from the buffer circuit using the external processor while performing the write operation, wherein the first data contains instruction code for the processor; and
 - monitoring the write operation with the external processor in response to the instruction code.
2. The method of claim 1, wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.
3. The method of claim 1, further comprises reading third data from a second array bank with a second external processor while performing the write operation.
4. The method of claim 1, wherein copying first data to the buffer circuit is automatically performed by the control circuitry in response to an externally provided write command.
5. The method of claim 1, wherein copying first data to the buffer circuit is performed in response to an externally provided command from the external processor.
6. A method of operating a flash memory comprising:
 - copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to a command from an external processor coupled to the flash memory;

performing a write operation to write second data to a second row of the first array bank using the external processor in response to a write command provided by the processor;

reading the first data from the buffer circuit using the external processor while performing the write operation in response to a read command provided by the processor, wherein the first data contains instruction code for the external processor; and

monitoring a status register of the flash memory with the external processor in response to the instruction code.

7. The method of claim 6, further comprises reading third data from a second array bank with a second external processor while performing the write operation.

8. The method of claim 6, wherein copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to a command from an external processor coupled to the flash memory further comprises copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to an externally provided write command from an external processor coupled to the flash memory.

9. A method of operating a flash memory comprising:
receiving a write command at the flash memory, wherein the write command is provided by an external processor coupled to the flash memory;
automatically copying first data stored in a first row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to the write command;
performing a write operation to write second data to a second row of the first array bank using the external processor in response to a write command provided by the processor;

reading the first data from the buffer circuit using the external processor while performing the write operation in response to a read command provided by the external processor, wherein the first data contains instruction code for the external processor; and

monitoring a status register of the flash memory with the external processor in response to the instruction code.

10. The method of claim 9, further comprises reading third data from a second array bank with a second external processor while performing the write operation.
11. A method of operating a synchronous flash memory comprising:
storing instruction code in each of a plurality of array blocks of the synchronous flash memory; and
copying the instruction code from a first array block to a buffer circuit using control circuitry of the memory, during a write operation, to the first array block using an external processor coupled to the memory so that the instruction code can be read from the buffer circuit using the external processor during the write operation.
12. The method of claim 11, wherein the synchronous flash memory comprises four array blocks.
13. The method of claim 11, wherein copying the instruction code is performed in response to an externally provided write command.
14. A method of operating a flash memory comprising:
copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory;
performing a write operation to write second data to the first array bank in response to an external processor coupled to the flash memory; and

reading the first data from the buffer circuit using the external processor while performing the write operation, wherein the first data contains instruction code for the processor.

15. The method of claim 14, further comprising monitoring the write operation with the external processor in response to the instruction code.
16. The method of claim 15, wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.
17. The method of claim 14, further comprises reading third data from a second array bank with a second external processor while performing the write operation.
18. The method of claim 14, wherein copying first data to the buffer circuit is automatically performed by the control circuitry in response to an externally provided write command.
19. The method of claim 14, wherein copying first data to the buffer circuit is performed in response to an externally provided command from the external processor.
20. A method of operating a flash memory comprising:
copying first data stored in a row of a first array bank to a buffer circuit using control circuitry of the flash memory in response to an external command;
performing a write operation to write second data to the first array bank; and
reading the first data from the buffer circuit while performing the write operation.
21. The method of claim 20, wherein performing a write operation to write second data to the first array bank further comprises performing a write operation to write

second data to the first array bank in response to an external processor coupled to the flash memory.

- 22. The method of claim 21, wherein reading the first data from the buffer circuit while performing the write operation further comprises reading the first data from the buffer circuit while performing the write operation, wherein the first data contains instruction code for the processor.
- 23. The method of claim 22, further comprising monitoring the write operation with the external processor in response to the instruction code.
- 24. The method of claim 23, wherein monitoring the write operation comprises performing a loop read operation of a status register of the flash memory.
- 25. The method of claim 20, further comprises reading third data from a second array bank while performing the write operation.
- 26. The method of claim 25, wherein reading third data from a second array bank while performing the write operation further comprises reading third data from a second array bank with a second external processor while performing the write operation.
- 27. The method of claim 20, wherein copying first data to the buffer circuit is automatically performed by the control circuitry in response to an externally provided write command.
- 28. The method of claim 20, wherein copying first data to the buffer circuit is performed in response to an externally provided command from an external processor.